		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY DOCKET NO.		SERIAL NO.			
Form PTO 1449 (Modified)				244838US2S		New Application			
				APPLICANT TO THE PROPERTY OF T					
LIST OF	REFER	RENCES CITED BY AF	PLICANT	Takashi YAMADA, et al.					
				FILING DATE		GROUP			
				Herewith					
				U.S. PATENT DOCUMENTS					
EXAMINER	,	DOCUMENT	DATE	NAME CLASS		SUB			
INITIAL		NUMBER	DATE			CLASS IF APPROPRIA		PPROPRIATE	
Ci /	AA	6,531,754	03/11/03	Hajime NAGANO, et al.					
an	AB	6,630,714	10/07/03	Tsutomu SATO, et al.					
	AC				<u> </u>				
	AD				ļ				
	AE				ļ				
	AF				ļ	ļI			
	AG		/	1	1				
	AH				<del> </del>				
	Al		1/_						
	AJ				ļ				
	AK		4						
	AL	-							
			FC	REIGN PATENT DOCUMENTS					
		DOCUMENT NUMBER	DATE	COUNTRY	łY		TRANSLATION YES NO		
a/	AM	10-303385	11/13/98	Japan				, x	
w	AN	8-316431	11/29/96	Japan				x	
co	AO	7-106434	04/21/95	Japan		<u> </u>		X	
on	AP	11-238860	08/31/99	Japan				x	
on	AQ	2000-91534	03/31/00	Japan				х	
CI	AR	2000-243944	09/08/00	Japan				X	
on	AS	8-17694	01/19/96	Japan				×	
a	AT	11-17001	01/22/99	Japan		<u></u>		X	
				(Including Author, Title, Date, Pertine					
a	AU	Robert HANNON, et TECHNOLOGY DIG	Robert HANNON, et al., "0.25 µm Merged Bulk DRAM and SOI Logic using Patterned SOI", SYMPOSIUM ON VLSI TECHNOLOGY DIGEST OF TECHNICAL PAPERS, 2000, pgs. 65-67						
on	AV	H. L. HO, et al., "A 0.13 µm High-Performance SOI Logic Technology with Embedded DRAM for System-On-A-Chip Application", IEDM TECH. DIG., 2001, pgs. 503-506							
	AW	T. YAMADA, et al., "An Embedded DRAM Technology on SOI/Bulk Hybrid Substrate Formed with SEG Process for High- End SOC Application", SYMPOSIUM ON VLSI TECHNOLOGY DIGEST OF TECHNICAL PAPERS, 2002, pgs. 112-113							
a	}	Hajime NAGANO et al. "SOI/Bulk Hybrid Wafer Process Using SEG (Selective Epitaxial Growth) Technique for High-End							
an	AX	DEVICES AND MAT	Soc Applications", EXTENDED ABSTRACTS OF THE 2002 INTERNATIONAL CONFERENCE ON SOLID STATE DEVICES AND MATERIALS, 2002, pgs. 442-443  Takashi YAMADA, et al., "An Embedded DRAM Technology in SOI for High-End Soc Application", SEMI TECHNOLOGY						
cn	AY	SYMPOSIUM, 2002, pgs. 2-39-2-44 (with English Abstract)							
	AZ				Ad Ad	Additional References sheet(s) attache			
Examiner		(/0	$\subseteq$			Date Considered 1-18-05			
*Examiner:	Initial if e and r	reference is considere not considered. Include	d, whether or n	ot citation is in conformance with MPEP m with next communication to applicant.	609; Draw	line throug	h citatio	n if not in	